CLAIMS

1. A phase locked loop circuit characterized by comprising:

a first feedback circuit operatively responsive to receipt of a first clock signal for generating a second clock signal synchronized in phase with the first clock signal; and

a second feedback circuit for generation of said second clock signal substantially equal in frequency to said first clock signal as input thereto.

2. The phase locked coop circuit as recited in claim 1, characterized in that said second feedback circuit includes a first converter circuit for conversion of said first clock signal into a first current, a second converter circuit for conversion of said second clock signal to a second current, and a current adder circuit for adding said first current and said second current together.

3. The phase locked coop circuit as recited in claim 1, characterized in that said second feedback circuit includes a first converter circuit for conversion of said first clock signal to a first voltage, a second converter circuit for conversion of said second clock signal to a second voltage, and a voltage adder circuit for adding said first current and said second current together.

4. A phase locked coop circuit characterized by

comprising:

a first control signal generator unit responsive to receipt of an input signal for generating a first control signal for integral control of an output signal;

a second control signal generator unit for generating based on the input signal a second control signal for proportional control of an output signal; and

an oscillator responsive to the first and second control signals for outputting a clock signal.

5. The phase locked coop circuit as recited in claim 4, characterized in that said first control signal generator unit uses a difference in phase between said input signal and said output signal to generate said first control signal whereas said second control signal generator unit uses a difference in frequency between said input signal and said output signal to generate said second control signal.

6. The phase locked coop circuit as recited in claim 4 or 5, characterized in that said first control signal generator unit includes a first converter circuit for conversion of an input signal to a first current, a second converter circuit for conversion of an output signal to a second current, and a current adder circuit for adding together said first current and said second current.

7. The phase locked coop circuit as recited in claim 4 or 5, characterized in that said first control

signal generator unit includes a first converter circuit for conversion of an input signal to a first voltage, a second converter circuit for conversion of an output signal to a second voltage, and a voltage adder circuit for adding together said first voltage and said second voltage.

8. The phase locked coop circuit as recited in claim 6, characterized in that the first and second converter circuits include a charging/discharging circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits folded for connection together.

9. An information processing apparatus characterized by comprising:

a clock generator unit including a first control signal generator unit for generation of a first control signal based on a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal based on a difference in frequency between an input signal and an output signal, and an oscillator for generation of a clock signal based on said first control signal and said second control signal;

a clock control unit for controlling the clock signal as output from said clock generator unit; and

a logic unit for processing data based on the clock

signal as generated by said clock generator unit.

10. The information processing apparatus as recited in claim 9, characterized in that said clock control unit is operable to control the clock signal as generated from said clock generator unit on the basis of a control signal as externally supplied thereto.

11. An information processing apparatus characterized by comprising:

a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input thereto and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input thereto;

a clock control unit for controlling the first clock signal as input to said clock generator unit; and

a logic unit for processing data on the basis of said second clock signal.

12. The information processing apparatus as recited in claim 11, characterized in that said clock control unit controls said first clock signal on the basis of a control signal as externally supplied thereto.

13. An information processor apparatus characterized by comprising:

a clock generator unit including a first feedback circuit for generation of a second clock signal synchronized in phase with a first clock signal as input

thereto and a second feedback circuit for generation of said second clock signal identical in frequency to said first clock signal being input;

a plurality of circuits operable based on the second clock signal as output from said clock generator unit; and

an interface for transmission of said second clock signal to more than one circuit selected from among said plurality of circuits being operable with a power supply different from that of said clock generator unit.

14. An information processing system having information processing apparatus for data processing based on a clock frequency and circuitry connected to said information processing apparatus for outputting an internal state, characterized in that

said information processing apparatus renders variable a clock frequency based on the internal state as output from said peripheral circuitry.

15. The information processing system as recited in claim 14, characterized in that said information processing apparatus includes a first control signal generator unit for generation of a first control signal from a phase difference between an input signal and an output signal, a second control signal generator unit for generation of a second control signal from a difference in frequency between an input signal and output signal, and an oscillator for outputting a clock

signal on the basis of said first control signal and said second control signal.

16. The information processing system as recited in claim 14, characterized in that said information processing apparatus includes a first feedback circuit for use in generating a second clock signal synchronized in phase with a first clock signal as input thereto, and a second feedback circuit for generation of said second clock signal synchronized in frequency with said first clock signal as input thereto.

17. The information processing system as recited in claim 14, 15 or 16, characterized in that said peripheral circuitry renders variable the clock frequency on the basis of a remaining amount of said power supply circuit.

18. A current switch circuit characterized by comprising:

a current switch with a control electrode forward-biased; and

a complementary output voltage switch for use in driving said current switch, said voltage switch having an output connected to a low voltage potential-side electrode of said current switch.

19. The current switch circuit as recited in claim 18, characterized in that said current switch is for constitution of a constant current circuit operable to turn on permitting flow of a constant current.

20. The current switch circuit as recited in claim

18 or 19, characterized in that said voltage switch has a power supply-side electrode coupled to a power supply via a voltage drop means.

21. The current switch circuit as recited in claim 18 or 19, characterized in that said voltage switch is connected at its output to an amplitude adjustment means.

22. The current switch circuit as recited in claim 18 or 19, characterized in that said current switch is a MOS transistor.

23. The current switch circuit as recited in claim 18 or 19, characterized in that said voltage switch is a CMOS inverter.

24. A phase locked loop circuit having a phase comparator circuit for outputting a phase difference signal from any one of two output terminals in accordance with a phase difference between two signals as input thereto, a charge pump circuit responsive to receipt of the phase difference signal from said phase comparator circuit for permitting charging and discharging of a capacitor to generate a control voltage signal, and an oscillator responsive to the control voltage signal from said charge pump circuit for adjusting a transmission frequency, characterized in that

said charge pump circuit includes a first current switch circuit for charging up said capacitor in deference to the phase difference signal as output from

one output terminal of said phase comparator circuit, and a second current switch circuit for discharging said capacitor in response to the phase difference signal as output from a remaining one of the output terminals of said phase comparator circuit, and

said first and second current switch circuits comprise a current switch with a control electrode forward-biased and a complementary paired output voltage switch for driving said current switch with an output connected to a low voltage-side electrode of said current switch.

25. A digital-to-analog converter circuit having a plurality of current switch circuits as provided in a way corresponding to respective ones of bits MLB-LSB of an input digital signal, characterized in that each of said plurality of current switch circuits comprises:

a current switch with a control electrode forward-biased;

a complementary output voltage switch for driving said current switch with an output of said voltage switch connected to a low voltage-side electrode of said current switch; and

said current switch being applied binary weighting to thereby permit flow of a current pursuant to bits of a signal as input to said voltage switch.

26. The phase locked loop circuit as recited in claim 7, characterized in that said first and second converter circuits include a charging/discharging

circuit having a capacitor and a CMOS inverter for performing charging and discharging on the basis of a signal as input thereto, and a current mirror filter with a plurality of current mirror circuits connected together in a folded fashion.

27. The current switch circuit as recited in claim 20, characterized in that said current switch is a MOS transistor.

28. The current switch circuit as recited in claim 20, characterized in that said voltage switch is a CMOS inverter.

29. The current switch circuit as recited in claim 21, characterized in that said current switch is a MOS transistor.

30. The current switch circuit as recited in claim 21, characterized in that said voltage switch is a CMOS inverter.

31. The current switch circuit as recited in claim 22, characterized in that said voltage switch is a CMOS inverter.